Design and Implementation of Brushless Motor Controller Based on SOPC

Qi Hui*. Liu Qingqiang.*

**Beijing University of Technology, Beijing, 100022*
China (Tel: 086-010-67390681; e-mail: l_qingqiang@ emails.bjut.edu.cn).

Abstract: In this paper, a kind of design of BLDM (Brushless DC motor) controller based on SOPC (System on programmable chip) is introduced. CPU, BLDM switching, PWM generator, and data acquisition module are integrated in a single FPGA chip. This design improves the integration, anti-interference and makes the system easy to promote. Experiment result has proved that the steady and dynamic performance of BLDM controller based on SOPC is so good meet the requirement of servo-system.

Key words: BLDCM; FPGA; SOPC; Servo-system;

1. INTRODUCTION

IN BLDM, electronic commutator is utilized to replace the mechanical brush and mechanical commutator which not only has the advantages of DC motor but also has the characteristics of simple structure, reliable operation, and maintenance-free of AC motor. Therefore it is widely applied in different circumstances. In this paper a design of BLDM controller based on SOPC is presented, in which CPU, dedicated hardware algorithm unit, PWM generator and data acquisition and processing unit are integrated on a single chip.

2. BASIC PRINCIPLE OF BLDCM CONTROL

BLDM is a typical motor of electromechanical integration and an entire BLDM control system is composed of 3 parts including motor body, rotor position sensor and the electronical switching circuit. BLDM commonly utilize a position sensor to detect rotational position and shutoff the transistor in three-phase Inverter Bridge by order to obtain the rotating magnetic filed synchronous with the rotor for the continuous operation of motor. In this design the brushless motor's rated power is 300W and the maximum speed is 3000 r/m. The commutation control table is made according the characteristics of motor and the 6-ladder waveform implemented by electronical commutator is shown in Fig, 1. In this figure H1, H2 and H3 are the Hall signals. PWM1~PWM6 are the shutoff signals of transistor in the inverter. And the transistor control signals changes every 60 electrical degrees and a period is divided into 6 states.

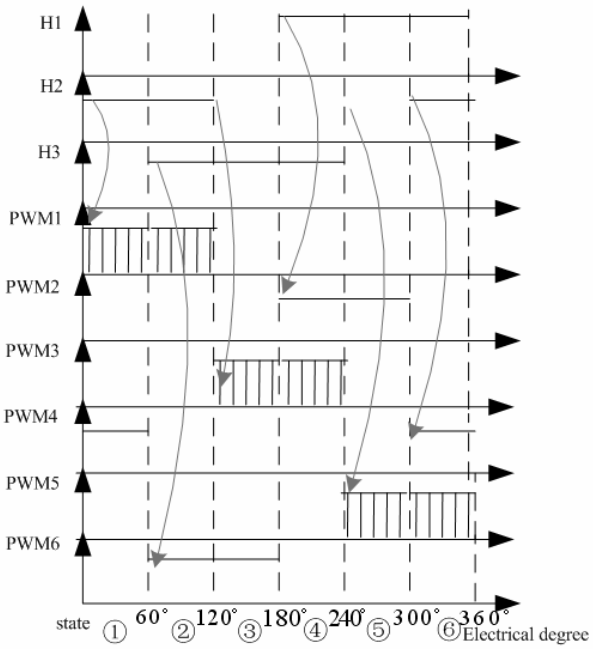
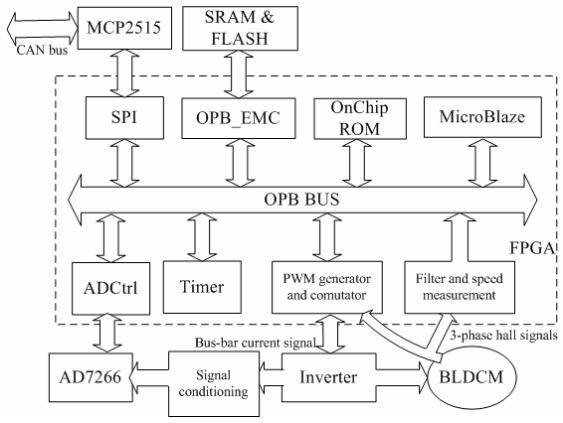


Fig.1.6-ladder waveform converted by 3-phase position signal

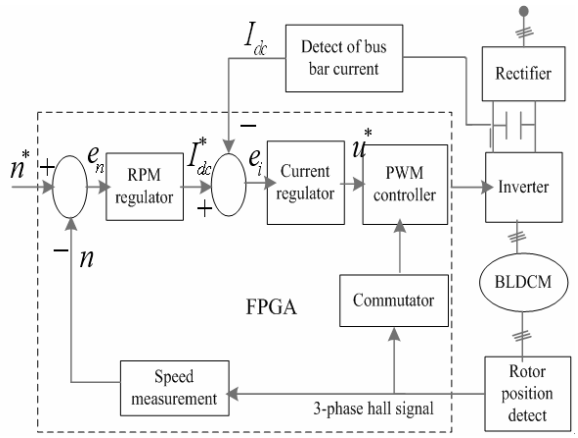
3. SYSTEM COMPONENTS

The whole control system is composed of central controller, inverter, signal acquisition and conditioning. Highly costeffective Spartan-3 FPGA chip acts as the central controller and the embedded 32-bit soft processor MicroBlaze acts as CPU integrated in FPGA. In the design of inverter, according to the actual load the motor drive chip IR2132 and power device IRFP250 are selected. The signal acquisition and conditioning are responsible for the acquisition and processing of the real-time data of motor operation which is then transmitted to the FPGA controller.

The whole system uses the control strategy of dual-loop of speed and current The whole system take the MicroBlaze processor as the control core and other peripherals are PWM waveform generator and commutation module, AD controller, speed measurement module and CAN communication module which makes the system have network function. The whole hardware structure and system control diagram are shown as Fig.2.



A. System hardware structure



B. System Control diagram

Fig.2 System hardware structure and control diagram

3. IMPLEMENTATION OF SYSTEM MODULES ON FPGA CHIP

3.1 PWM waveform generator and the commutation module

There are three kinds of PWM modulation including width-fix and frequency-adjust, width-adjust and frequency-fix and width-adjust and frequency-adjust. In this design, considering the flexibility in the actual application the third method is selected. The PWM generator and commutation module is shown as Fig.3. In this figure the PWM period is changed by set period and the period comparator. The PWM waveform is generated by the pulse width value assigned by CPU and pulse width comparator. And then the PWM wave-form is sent to the Commutator and signal output control module. Blocking signal is used for shut-off of driving signal when the system breaks down.

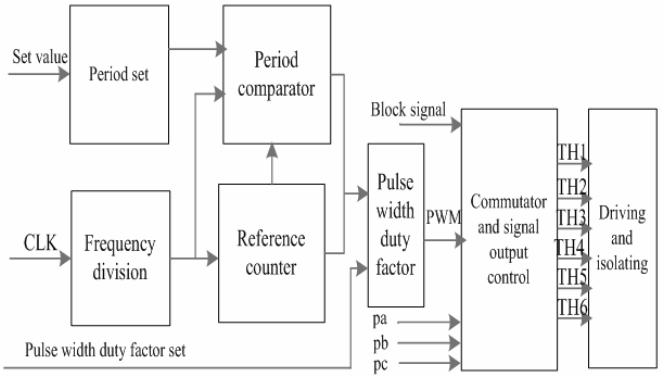


Fig.3. PWM generator and commutation module

3.2 Speed measurement and Hall signal filter

Speed measurement module is implemented by the counter in master clock every Hall signal cycle. The speed measurement formula is as below,

$$Speed = 60/Ts * CNT * i \quad (1)$$

In (1), Ts indicates master clock. CNT indicates the counter value in the Timer module. i indicates the number of pole pairs of motor. The division computation in the speed measurement is implemented by hardware logic form. The division IP core is available by the Core Generator Tool in ISE from Xilinx Company. This gives CPU a coprocessor which not only improves the system operation efficiency but also makes the computation more accurate and stable. It must be noted that Hall signals in poor conditions susceptible to interference with other signals which has great impact on the accuracy of speed measurement. So the Hall signals digital filter is needed. In the design of filter, three consecutive 1 is defined as 1 and three consecutive 0 is defined as 0, but not all of 3 consecutive 1 or 0 is defined as interference signal. The Verilog source code for the Hall signals digital filter is as below,

```
reg d0,d1,d2；//Delay registers

reg pa；//Hall signal pa；

always @(posedge clk ) begin

  d0<=pa;

  d1<=d0;

  d2<=d1;

  pa<=(d0 & d1 & d2) or ( (d0 | d1 | d2) & pa );

end
```

BLDM commutation and the speed measurement module are simulated by Modelsim and the simulation waveform is

shown as Fig.4. In the figure, the 6-road control transistor signals Th1, Th2, Th3, Th4, Th5 and Th6 are from pa, pb and pc Hall signals by commutation. When the velocity of motor changes or the Hall signal period changes, the speed value changes accordingly. When load_speed signal is high, MicroBlaze can read the speed value by OPB bus.

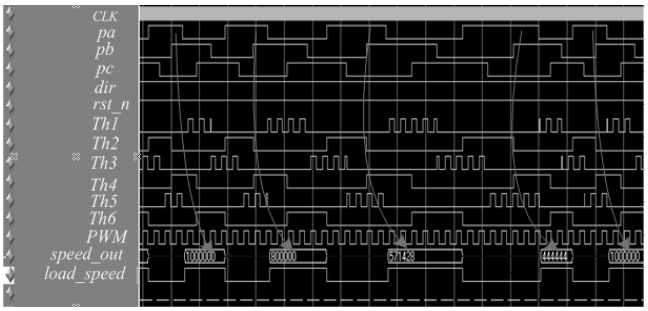


Fig.4. BLDM commutation and speed measurement module simulation waveform

3.3 AD controller

Considering the actual sampling frequency and accuracy, select AD7266 is selected for real-time data acquisition. And the main properties of this AD are as follows, dual 12-bit, 3 channels ADC, 2 MSP throughput rate, and accurate on-chip reference voltage. In this design the two input signals are current signal and the system temperature signal. The data converted by AD is firstly shifted 2 bit to the left. And then carry on average filter for every 8 groups of data. In FPGA, the average filter is easy to implement by shift and addition. Fig.5 is the experimental waveform of AD real-time data in the oscilloscope. In the waveform there are 32 bits between two chip select signals which includes two-road serial data. The serial data is converted into parallel data which is stored in the buffer and then the parallel data is transmitted to MicroBlaze by OPB bus.

3.4 Other system module

There are many IP cores for free supplied by embedded development tool EDK from Xilinx Company and the software driver for IP cores are also supplied which are very helpful and flexible for users. In the design the main IP cores used for free are UART, external memory controller and SPI controller. The SPI controller is used for the CAN communication for MCP2515 and the data is read and write in the buffer in MCP2515 by SPI communication.

4. SYSTEM SOFTWARE DESIGN

Xilinx Company provides SDK tool integrated in EDK suit for the software development users which can generate the software driver automatically according to the hardware structure defined by the user. Then the user can develop the software system flexibly on the basis of the software driver. There are two parts in the software design, the CAN communication and the dual-loop control of BLDM. The CAN communication implements the transmission and receiving of message between BLDM controller and other CAN nodes. In the design of dual-loop control including current and speed regulation only one timer interrupt is used for the efficiency of program execution. In the interrupt service program, when new message is detected from CAN bus the given command word is updated and the dual-loop regulation is implemented according to the given command word and the feedback information. Fig.6 is the system software flow.

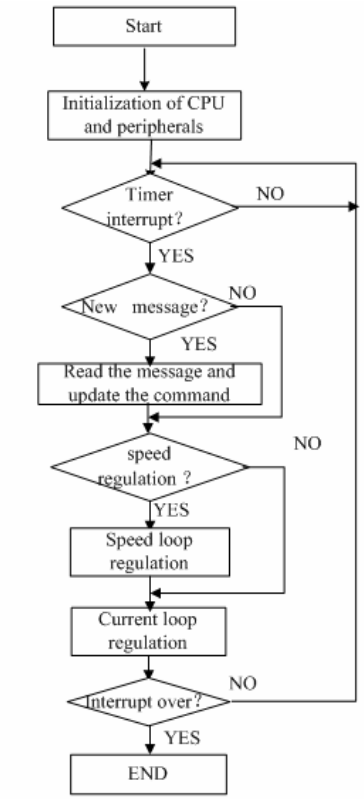


Fig.6. the system software flow

5. CONCLUSION

This paper introduces a design and implementation of BLDM controller based on SOPC technology in FPGA. The system core controller and the main peripherals are integrated in a single FPGA chip which reduced the system volume, conformed to the entire digital and modulation trend of motion control development. The experimental waveform of PWM modulation and commutation is shown as Fig.7. The experiment result indicated that the speed of BLDM is steady in 0~3000r/m scope, the step response is less than 100ms and the overshoot of speed is less than 2%.

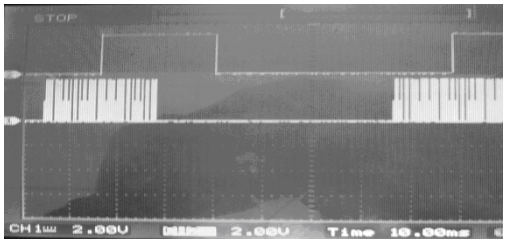


Fig.7 The experimental waveform of commutation and PWM modulation

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